The Stackup Legend below this is static.
If you change the stackup, update the Legend.

Layer Stack Up Detail for: Ref_Design.PcbDoc

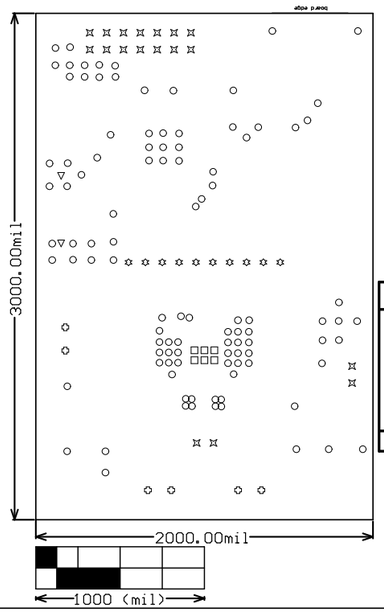
Layer Name	Gerber Document	Copper Thickness	Dielectric Material
Top Solder Mask	(.GTS)		Solder Resist
Top Layer	(.GTL)	2.8mil	FR-4
Bottom Layer	(.GBL)	2.8mil	
Bottom Solder Mask	(.GBS)		Solder Resist

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
3450MIL X 4950MIL

Number of Layers : 2
MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 8 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
COPPER THICKNESS (FINISHED):
OUTER: [ ] 1.4MIL (1oz) [ ] 2MIL (1.4oz) [X] 2.8MIL (2oz)
INNER SIGNAL: [ ] 1.4MIL (1oz) [ ] 2.8MIL (2oz) [X] N/A
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER _____
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR:
[X] GREEN [ ] BLUE [ ] OTHER _____
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [ ] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK



Symbol	Hit Count	Tool Size	Plated	Hole Type
□	6	12.992mil (0.33mm)	PTH	Round
○	103	15mil (0.381mm)	PTH	Round
✡	10	38mil (0.965mm)	PTH	Round
⌑	18	40mil (1.016mm)	PTH	Round
▽	2	47.244mil (1.2mm)	PTH	Round
✪	6	50mil (1.27mm)	PTH	Round
	145 Total			

Drill Table

TEXAS INSTRUMENTS

PROJECT TITLE: DRV8848EVM
DESIGNED FOR: Public Release
FILE NAME: DRV8848EVM.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: DRV8848EVM	REV: REV A	SVN REV: Not In VersionControl
LAYER NAME = [illegible]sions			
PLOT NAME = Fabrication Drawing	GENERATED : 9/11/2014 8:38:10 AM	TEXAS INSTRUMENTS	

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ENGINEER:	LAYOUT BY:
Anda zhang	Anda zhang
SCALE: 1.10	ALTIUM DESIGNER VERSION: 10.0.0.27009